

new/usr/src/uts/i86pc/io/amd\_iommu/amd\_iommu\_acpi.h

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*****
7617 Sat Dec 9 08:30:39 2017
new/usr/src/uts/i86pc/io/amd_iommu/amd_iommu_acpi.h
8902 Panic with debug kernel on AMD Ryzen hardware
*****
1 /*
2  * CDDL HEADER START
3  *
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16 * fields enclosed by brackets "[]" replaced with your own identifying
17 * information: Portions Copyright [yyyy] [name of copyright owner]
18 *
19 * CDDL HEADER END
20 */
21 /*
22 * Copyright 2017 Gary Mills
23 * Copyright (c) 2009, 2010, Oracle and/or its affiliates. All rights reserved.
24 */

26 #ifndef _AMD_IOMMU_ACPI_H
27 #define _AMD_IOMMU_ACPI_H

29 #ifdef __cplusplus
30 extern "C" {
31 #endif

33 #include <sys/sunddi.h>
34 #include <sys/acpi/acpi.h>
35 #include <sys/acpica.h>
36 #include <sys/amd_iommu.h>
37 #include "amd_iommu_impl.h"

39 #ifdef _KERNEL

41 #define IVRS_SIG          "IVRS"

43 /*
44  * IVINFO bit fields
45  * Documented at: http://support.amd.com/TechDocs/48882\_IOMMU.pdf
46  * IVINFO settings
47  */
47 #define AMD_IOMMU_ACPI_IVINFO_RSV1      (31 << 16 | 23)
48 #define AMD_IOMMU_ACPI_HT_ATSRSV       (22 << 16 | 22)
49 #define AMD_IOMMU_ACPI_VA_SIZE          (21 << 16 | 15)
50 #define AMD_IOMMU_ACPI_PA_SIZE          (14 << 16 | 8)
51 #define AMD_IOMMU_ACPI_GVA_SIZE         (7 << 16 | 5)
52 #define AMD_IOMMU_ACPI_IVINFO_RSV2     (4 << 16 | 1)
53 #define AMD_IOMMU_ACPI_IVINFO_EFRSUP   (0 << 16 | 0)
49 #define AMD_IOMMU_ACPI_IVINFO_RSV2     (7 << 16 | 0)

55 /*
56  * IVHD Device entry len field
57  */
58 #define AMD_IOMMU_ACPI_DEVENTRY_LEN     (7 << 16 | 6)
```

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60 /*
61  * IVHD flag fields definition
62  */
63 #define AMD_IOMMU_ACPI_IVHD_FLAGS_RSV      (7 << 16 | 5)
64 #define AMD_IOMMU_ACPI_IVHD_FLAGS_IOTLBSUP (4 << 16 | 4)
65 #define AMD_IOMMU_ACPI_IVHD_FLAGS_ISOC    (3 << 16 | 3)
66 #define AMD_IOMMU_ACPI_IVHD_FLAGS_RESPASSPW (2 << 16 | 2)
67 #define AMD_IOMMU_ACPI_IVHD_FLAGS_PASSPW  (1 << 16 | 1)
68 #define AMD_IOMMU_ACPI_IVHD_FLAGS_HTTUNEN (0 << 16 | 0)

70 /*
71  * IVHD IOMMU info fields
72  */
73 #define AMD_IOMMU_ACPI_IOMMU_INFO_RSV1     (15 << 16 | 13)
74 #define AMD_IOMMU_ACPI_IOMMU_INFO_UNITID  (12 << 16 | 8)
75 #define AMD_IOMMU_ACPI_IOMMU_INFO_RSV2    (7 << 16 | 5)
76 #define AMD_IOMMU_ACPI_IOMMU_INFO_MSINUM  (4 << 16 | 0)

78 /*
79  * IVHD deventry data settings
80  */
81 #define AMD_IOMMU_ACPI_LINT1PASS           (7 << 16 | 7)
82 #define AMD_IOMMU_ACPI_LINT0PASS          (6 << 16 | 6)
83 #define AMD_IOMMU_ACPI_SYSMGT             (5 << 16 | 4)
84 #define AMD_IOMMU_ACPI_DATRSV            (3 << 16 | 3)
85 #define AMD_IOMMU_ACPI_NMIPASS           (2 << 16 | 2)
86 #define AMD_IOMMU_ACPI_EXTINTPASS        (1 << 16 | 1)
87 #define AMD_IOMMU_ACPI_INITPASS          (0 << 16 | 0)

89 /*
90  * IVHD deventry extended data settings
91  */
92 #define AMD_IOMMU_ACPI_ATSDISABLED        (31 << 16 | 31)
93 #define AMD_IOMMU_ACPI_EXTDATRSV         (30 << 16 | 0)

95 /*
96  * IVMD flags fields settings
97  */
98 #define AMD_IOMMU_ACPI_IVMD_RSV           (7 << 16 | 4)
99 #define AMD_IOMMU_ACPI_IVMD_EXCL_RANGE    (3 << 16 | 3)
100 #define AMD_IOMMU_ACPI_IVMD_IW           (2 << 16 | 2)
101 #define AMD_IOMMU_ACPI_IVMD_IR           (1 << 16 | 1)
102 #define AMD_IOMMU_ACPI_IVMD_UNITY        (0 << 16 | 0)

104 #define AMD_IOMMU_ACPI_INFO_HASH_SZ       (256)

106 /*
107  * Deventry special device "variety"
108  */
109 #define AMD_IOMMU_ACPI_SPECIAL_APIC       0x1
110 #define AMD_IOMMU_ACPI_SPECIAL_HPET       0x2

112 typedef enum {
113     DEVENTRY_INVALID = 0,
114     DEVENTRY_ALL = 1,
115     DEVENTRY_SELECT,
116     DEVENTRY_RANGE,
117     DEVENTRY_RANGE_END,
118     DEVENTRY_ALIAS_SELECT,
119     DEVENTRY_ALIAS_RANGE,
120     DEVENTRY_EXTENDED_SELECT,
121     DEVENTRY_EXTENDED_RANGE,
122     DEVENTRY_SPECIAL_DEVICE
123 } ivhd_deventry_type_t;
unchanged_portion_omitted
```